Technical Progress Report 2/01/93 - 05/01/93
Construction of a Connectionist Network Supercomputer
University of California, Berkeley
ONR URI Grant No. N00014-92-J-1617

1 Introduction

This quarter marks the end of the first year of funding by the ONR for the CNS-1 project. With the architecture of the machine at a stable state, work during the quarter focused on design and engineering details at the silicon, software, and system levels.

2 Technical Status

2.1 VLSI design

During the past few months the core VLSI design team has been implementing the first *Torrent* processor, T0, using a mixture of full custom and standard cells in 1.2 micron CMOS. The design of the T0 processor is expected to be complete in early July. The chip will be approximately 14 mm on a side, and is targeted to run at 50 MHz. This design represents a significant step towards the design of the T1 processor to be used in the CNS-1 machines. The T1 design will begin this summer, starting from the T0 database.

2.2 System Packaging

We have continued to investigate the technology to be used for the CNS-1 Torrent module boards. Although several MCM (Multi-Chip Module) vendors have capabilities suitable for CNS-1, there remain many questions about reliability, repairability and price. These questions are not, however, unique to this project, and are the source of much industry activity.

Cooling of the CNS-1 processor modules has been one of the major design challenges in the physical design of the machine. A heat sink manufacturer has been commissioned to undertake a thermal design study using the configuration of the CNS-1 modules. He will produce sample heat sinks and generate test data from a scale model of the module.

2.3 Software

Software has progressed on many levels during the last quarter. On the low level, the work has centered on design support for the T0 processor team. An ISA simulator of the

architecture is nearly complete; the scalar unit portion of this ISA has been successfully verified by comparison with a MIPS 3000 chip. The interface specification connecting the ISA and other software support tools (debuggers, program generators, and other simulators) is also complete. Work continues on these support tools as well.

On a higher level, the CLONES simulation system, which is a primary tool of RAP machine users, has been redesigned for the CNS-1 system, and renamed BoB (Boxes of Boxes). Among BoB's new features is a new binary database format and an interface for extremely large data files. BoB will make it easier to map connectionist and non-connectionist algorithms onto the CNS-1. The machine will be subdivided into several SPMD (single program multiple data) machines that communicate by efficient buffered message passing. Any subgraph of the dataflow graph can be mapped onto one of these clusters of T0 processors.

Much of the software work related to CNS-1 came together at a workshop sponsored by ICSI, Adaptive Solutions and Siemens AG on April 19th and 20th at ICSI, called "Workshop on Software & Programming Issues for Connectionist Supercomputers." The two day event featured talks on software topics from simulators to supercomputers.

3 Publications and Talks

This section lists the recent publications and talks.

Appeared:

Lazzaro, J., Wawrzynek, J., "Evaluating Silicon Models of Spectral Shape," Neural Networks for Computing 1993, April 13-15, Snowbird Utah.

Morgan, N., "Making Useful Neurocomputers," Third International Conference on Microelectronics for Neural Networks, 6-8th April 1993 Edinburgh, Scotland.

Asanović, K., Beck, J., Feldman, J., Morgan, N., and Wawrzynek, J., "Development of a Connectionist Network Supercomputer," Third International Conference on Microelectronics for Neural Networks, 6-8th April 1993 Edinburgh, Scotland.

Asanović, K., Beck, Callahan, T., J., Feldman, J., Irissou, B., Kingsbury, B., Kohn, P., Lazzaro, J., Morgan, N., Stoutamire, D., and Wawrzynek, J., "CNS-1 Architecture Specification", technical report number TR-93-021, April 1, 1993.

To Appear:

Lazzaro, J., Wawrzynek, J., Mahowald, M., Sivilotti, M., and Gillespie, D. (1993). "Silicon auditory processors as computer peripherals," in *Advances in Neural Information Processing Systems 5*, San Mateo, CA: Morgan Kaufmann Publishers. *A longer version will appear Spring 1993 in* IEEE Transactions on Neural Networks.

Wawrzynek, J., Asanović, K., and Morgan, N., "The Design of a Neuro-Microprocessor," IEEE Transactions on Neural Networks, *to appear Spring 1993.*

Asanović, K., Morgan, N., and Wawrzynek, J., "Using Simulations of Reduced Precision Arithmetic to Design a Neuro-Microprocessor" Invited submission to Journal of VLSI Signal Processing, *to appear Spring 1993* in a special issue on Neural Networks, 1993.

Additional Public Talks:

J. Wawrzynek, "Development of a Connectionist Network Supercomputer," Industrical Liaison Program, 15th Annual Conference, UC Berkeley, March 10 & 11, 1993.

Beck, J., "CNS-1 Hardware Overview," Workshop on Software and Programming Issures for Connectionist Supercomputers, International Computer Science Institute, Berkeley, CA, April 19th and 20th.

4 Student Researchers

The CNS-1 project has had a significant effect on the education of graduate and undergraduate students at our institution. Below is a list of all students that have substantially interacted with the CNS-1 project. There are 11 Ph.D., 2 M.S., and 2 B.S. students associated with the project.

Name	Degree Goal	Expected Date	Current Research Topic
Krste Asanović	Ph.D.	1995	Computer Architecture for Neural Networks
David Bailey	Ph.D.	1997	User Interfaces for Neural Networks
Tim Callahan	Ph.D.	1998	Network Architectures for Parallel Machines
Joe Chung	B.S.	1993	Software Support for VLSI CAD
Benedict A. Gomes	Ph.D.	1997	Parallel Languages for Simulation
Randy Huang	B.S.	1993	VLSI Circuit and Layout of Custom Processors
Bertrand Irissou	M.S.	1993	High-Speed Techniques in VLSI Processors
Brian Kingsbury	Ph.D.	1995	Auditory Processing (Hardware and Algorithms)
Yochai Konig	Ph.D	1995	Speech Recognition on Parallel Machines
Sven Meier	M.S.	1994	Circuit Issues in High-Speed Signalling
Srini Narayanan	Ph.D.	1998	Parallel Languages for Simulation
Stylianos Perissakis	Ph.D.	1999	Circuit Issues in High-Speed Signalling
David Stoutamire	Ph.D.	1997	Parallel Languages for Simulation
Thorsten von Eicken	Ph.D.	1993	Efficient Communication in Parallel Machines
Su-Lin Wu	Ph.D.	1997	Mapping Sensory Algorithms on Parallel Machines